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Report (REP)

Measurements on the V791 board

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2. Introduction

This document contains the results of the measurements performed on the front-end electronics of the ICARUS experiment. The experimental set-up consisted of a V791 board, containing the preamplifiers and the digitizers, and the V789 module which hosts the trigger logic and the VME interface. Moreover, the document shows that the results and the methods adopted for the measurements agree with the contents of the Technical Specification Documents approved by all the members of this ICARUS collaboration during the project phase of the front-end electronics (SPT 00100/98:V791X.SPTX/00 and SPT 00100/98:V789X.SPTX/00 documents).

3. Experimental set-up

The experimental set-up is constituted by:

- Pulse generator (Philips, Mod. PM5715);
- Attenuator HP Mod. 8496A;
- VME crate with linear power supply and V430 backplane;
- Specially developed board for signal driving on the backplane;
- Specially developed board for the VME/PC Parallel Port;
- Personal Computer HP Mod. Vectra VL Pentium 120 MHz;
- Specially developed power supply for the V791 board;
- oscilloscope Tektronix Mod. TDS 520B (1Gs/s).

A trapezoidal-shaped pulse is sent to one of the 32 inputs of the V791 board after an appropriate attenuation. The figures 1, 2 and 3 show the pulse oscillograms at the three different attenuations used during measurements.

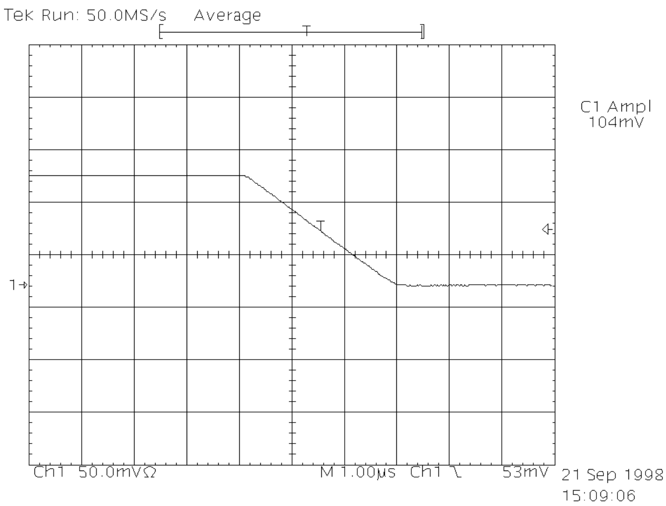

Fig.1 – Non attenuated input pulse

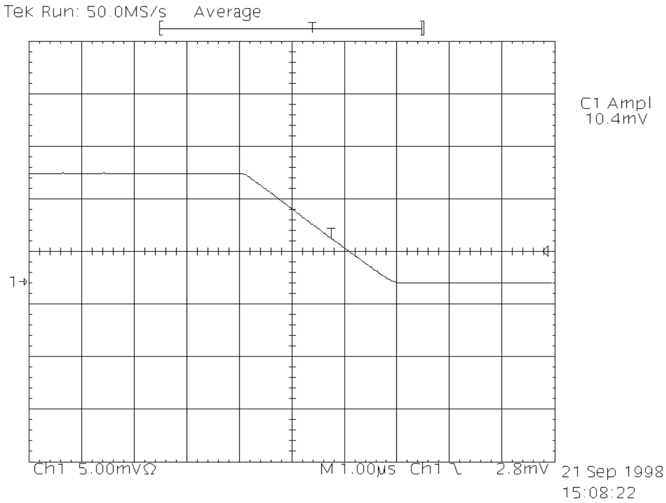

Fig.2 – 20 dB attenuated input pulse

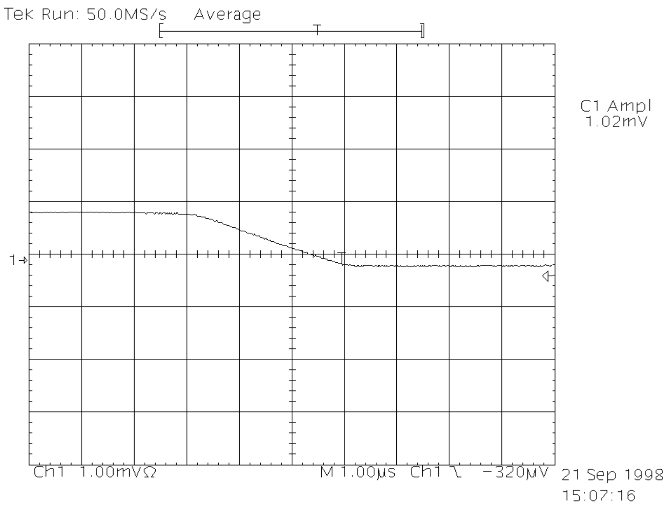

Fig.3 – 40 dB attenuated input pulse

The three attenuations chosen for the measurements are 0, 20 and 40 dB corresponding to about *300 fC*, *30 fC* and *3 fC*, respectively, since the signals are injected into the input of the preamplifiers through *3 pF* capacitance.

The digitised signals are sent to the memories contained in the V789 module through the LVDS serial link. The PC reads these memories via the parallel port connected to the VME interface board.

The set-up of the parameters and the data elaboration in real time are obtained by using a special software assembled in C language.

Two V791 boards, serial number 1 and 2, were used for the measurements. These two boards have the same components, except for the two FETs mounted on the channel 4 of the board n. 2 which are Philips BF861B-type FETs instead of Interfet IF4500-type FETs. Referring to figure 4 the values of the components are:

Rf = 5.6 MΩ
Cf = 0.17 pF
R1 = 27 KΩ
C1 = 39 pF
R2 = 470 Ω
C2 = 2.2 nF

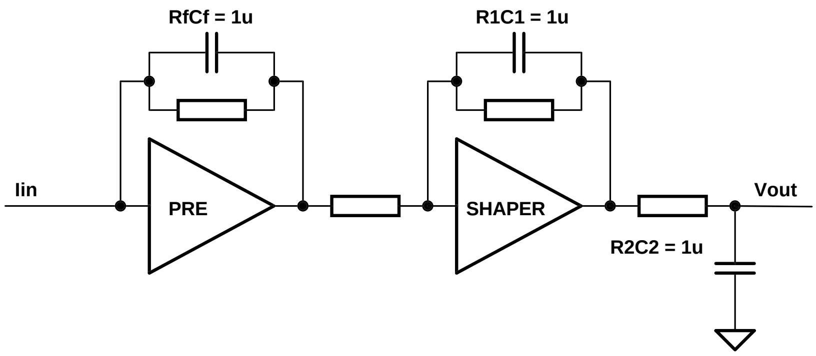

Fig.4 – Block diagram of the channel

4. Measurements of the analog channel and digitisation noise

This measurement was performed by connecting a shielded cable to the output of one of the shapers and by keeping in the RESET condition the digital section of the V791 board. The channel used is the channel 0 of the board n.2.

The purpose is to underline the effect of the digitisation on the output signal of the analog channel.

A *390 pF*-SMD ceramic capacitance soldered on the free pads reserved to the third J-FET was used in order to simulate the detector. During the test it has been noted that the use of SMD ceramic capacitance increases the noise with respect to the equivalent COG assembled in a traditional way. For the easiness of assembly SMD capacitances were used.

Figure 5 shows the trend of the noise at the output of the shaper with the relevant RMS value measured with the oscilloscope (*bandwidth = 20 MHz*).

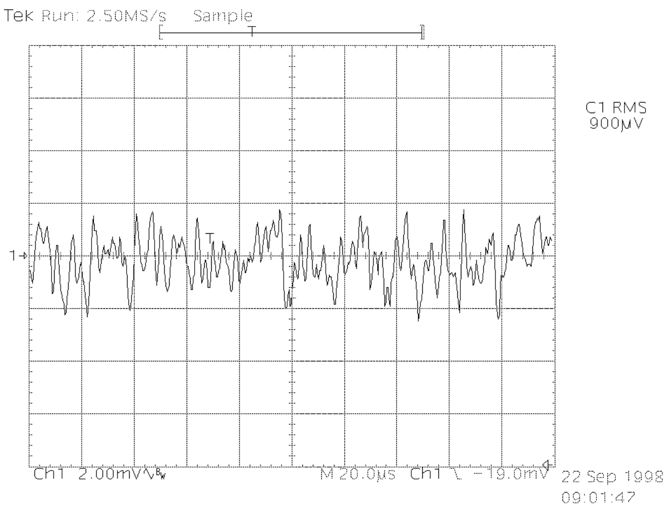

Fig.5 – Noise of the analog channel with *Cd = 390 pF*

It can be noted that the noise value measured is comparable both with the value indicated at page 14 of the document « *ICARUS AMPLIFIER* » by D. Favaretto and with that in « *ICARUS FRONT END ELECTRONICS* » by P. Cennini, A. Puccini. These documents are the annexes n.1 and n.2, respectively, of the V791 board Technical Specifications mentioned in the Introduction.

It is to be noted that the J-FETs used by D. Favaretto for the measurements (Toshiba 2SK371 components) have features equivalent to those of the components used for the V791 board (Interfet IF4500 components).

As will be described in the following Chapters, the noise of the channel itself after the digitisation is *1.01 count rms*. Taking into account that the measured gain of the analog-digital converter is *0.944 mV/count*, we obtain:

$$1.01 * 0.944 = 0.95 \ mV \ rms$$

The rms noise given by the digitiser can be roughly evaluated as follows:

$$V_{n\_digit} = (V^2_{n\_tot} - V^2_{n\_analog})^{1/2} = (0.95^2 - 0.90^2)^{1/2} = 0.304 \ mV_{RMS}$$

This corresponds to $0.32 \ count_{RMS}$, which is a value very near to that theoretically calculated ($12^{-1/2} = 0.29 \ count_{RMS}$).
The analog-digital converter has been designed in order to have a *0.94 mV/count* gain. For the channel under investigation this has been achieved with a good precision.
We can conclude that:

- **The noise of the analog channel fulfils the requirements stated in the Technical Specification documents.**
- **The noise given by the digitisation is negligible.**

5. Noise

Figures 6 and 7 show the software screen hardcopies with the results of the averages and standard deviations relative to all the channels. The measurements were performed by simulating the detector capacitances with *390-pF* SMD ceramic capacitors.

Every 100 acquisitions, controlled by a software trigger, 25600 samples per channel are acquired and then used to calculate the average and the standard deviation.

ch	media	dev	ch	media	dev
0	446.05	1.00	16	445.78	0.91
1	445.00	0.89	17	432.80	0.96
2	444.26	0.91	18	439.99	0.99
3	446.70	0.95	19	442.58	0.97
4	447.58	0.92	20	444.12	1.01
5	447.39	0.94	21	431.64	0.91
6	439.28	1.04	22	445.00	1.16
7	447.69	1.11	23	449.31	0.97
8	447.53	0.93	24	447.58	0.95
9	443.29	0.98	25	434.36	0.97
10	438.83	0.94	26	450.88	0.99
11	443.27	0.90	27	438.97	1.16
12	448.52	0.93	28	446.75	1.00
13	448.55	1.00	29	441.95	1.03
14	435.21	0.98	30	455.01	1.14
15	453.29	1.16	31	449.11	1.00

Fig.6 – Average ('media' in the figure) and standard deviation of the board n. 1

ch	media	dev	ch	media	dev
0	450.41	1.01	16	462.16	1.00
1	458.84	0.91	17	444.00	0.88
2	450.01	1.05	18	459.23	0.99
3	462.88	0.92	19	456.03	0.90
4	463.72	1.02	20	472.80	0.86
5	471.29	0.89	21	450.67	0.90
6	440.25	0.91	22	468.32	0.95
7	460.96	0.88	23	450.38	0.94
8	448.20	0.87	24	464.24	0.84
9	454.31	0.90	25	437.69	0.91
10	453.05	0.92	26	460.13	0.89
11	456.30	0.88	27	450.79	0.92
12	455.61	0.91	28	477.64	0.91
13	460.32	0.95	29	453.16	0.92
14	456.00	0.98	30	468.33	1.08
15	457.38	1.00	31	465.52	1.03

Fig.7 - Average ('media' in the figure) and standard deviation of the board n. 2

As can be seen in figure 8, which shows all the standard deviation values of the channels investigated, it is difficult to find a correlation between the channel number and the relevant noise level.

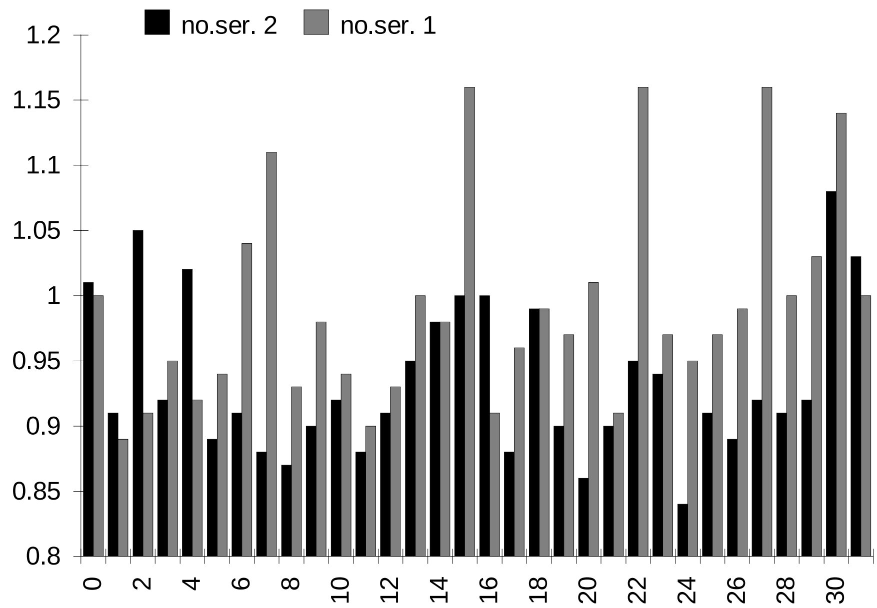

Fig.8 – Distribution of the standard deviations of the channels

The RMS noise of the channels is *0.96 counts ± 20%.*

6. Analysis of the output signals

This chapter contains the measurements made by sending the signals described in Chapter 3 to the input of the V791 board.

The figures 9, 10 and 11 show the oscillograms at the output of the shaper corresponding to the channel 0 of the board n.2. The three figures display the output when the input signal is maximum, medium and minimum, respectively. During the measurement the digital section was working and a capacitance (*Cd = 390 pF*) was used at the input of the channel.

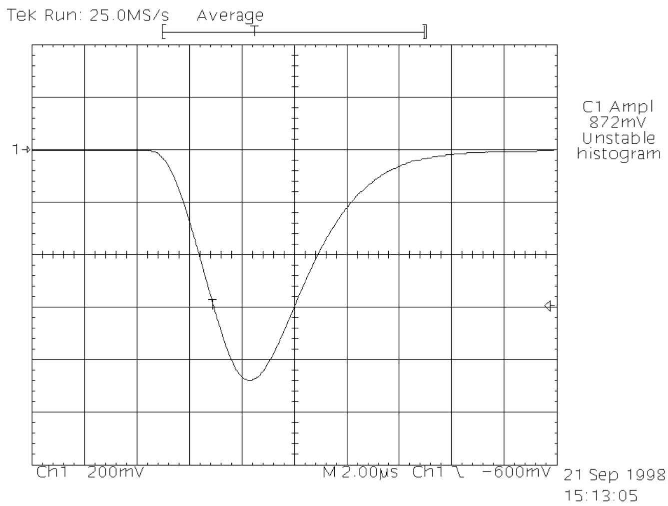

Fig.9 - – Analog output with *300 fC* input signal

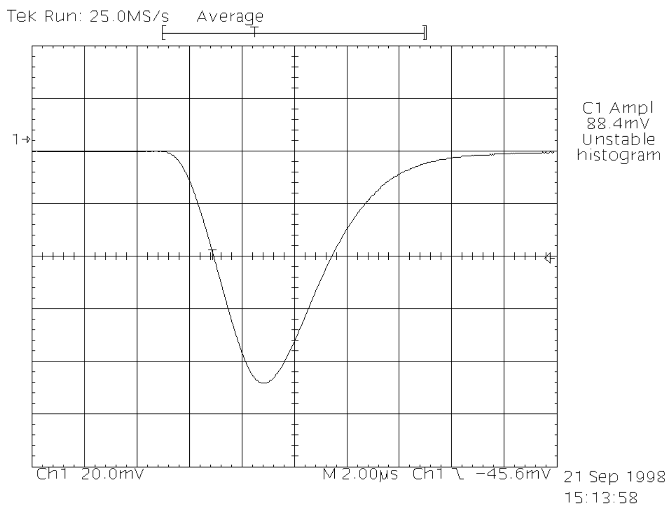

Fig.10 – Analog output with *30 fC* input signal

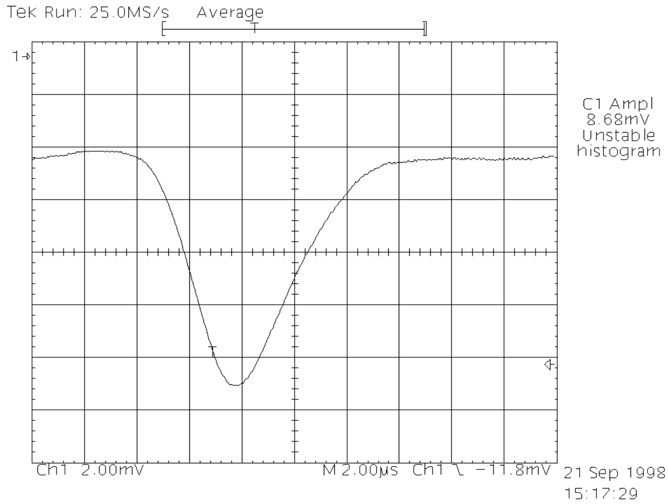

Fig.11 - Analog output with *3 fC* input signal

The signals themselves were acquired with the complete chain and elaborated with the software, the screens of which are displayed in the figures 12, 13 and 14.

The software programme, after each acquisition of data relative to the channel under investigation, applies a median filter to the signal and, on this basis, determines a trigger condition and timing. According to the detected trigger time the signal is integrated in order to obtain some particular statistics. Moreover, since the number of acquisitions is known, it is possible to calculate the trigger efficiency, i.e. the ratio between the number of acquisitions and the number of triggers detected via software. The programme shows three graphs and some parameters at a speed of up to 10 acquisitions per second.

The graph in the upper left is the oscillogram of the signal, the amplitude of which is scaled so as to be fully contained in the window. The measurement unit of the vertical axis are *counts*. The two vertical lines on both the sides of the pulse represent the integration area: this can be varied by modifying the parameters **pretrg** e **postrg** corresponding to the number of samples before and after the trigger, respectively, as indicated in the column on the right. The horizontal line in the graph marks the range of where the baseline is calculated. Also in this case the number of samples used and the value obtained is displayed in the column of the parameters.

The graph in the middle displays the signal after the median filter application. The vertical axis is equal to that of the previous graph. The vertical line represents the trigger time, determined on the basis of a threshold and a time of overthreshold.

The graph on the bottom shows the distribution of the values obtained from the integrations.

The parameters displayed in the column on the right are:

- **Channel (canale):** number of the channel analysed;
- **Median (mediano):** length of the filter;

- **Threshold (soglia):** trigger threshold;
- **Trigger width (largh. Trigger):** number of the samples above the threshold to generate a trigger;
- **Baseline length (lungh. Baseline):** number of samples on which the baseline is calculated;
- **pretrg:** number of samples for the integration before the trigger;
- **postrg:** number of samples for the integration after the trigger.

All the values of the parameters described above can be modified by means of a suitable menu. The values used are those that allow realistic measurements. Moreover, the right column reports the results of some special statistics:

- **trigger:** number of valid trigger signals and time of the last trigger;
- **Charge (carica):** value (in counts) obtained by integrating the signal amplitude calculated by subtracting the baseline from the actual values of the samples in the last acquisition;
- **stdev sum:** standard deviation of the charge averaged on the last 100 acquisitions;
- **mean sum:** average of the charge calculated on the last 100 acquisitions;
- **ENC:** Equivalent Noise Charge calculated by dividing the standard deviation of the charge by the mean charge and multiplying it by the number of electrons of the minimum signal (*3 fC = 18750*); the instantaneous values are averaged on the whole number of valid trigger signals; it has to be noted that **this datum is meaningful only if the input signal is relative to the minimum charge**;
- **delta:** peak value of the signal in the integration window decreased by the baseline.

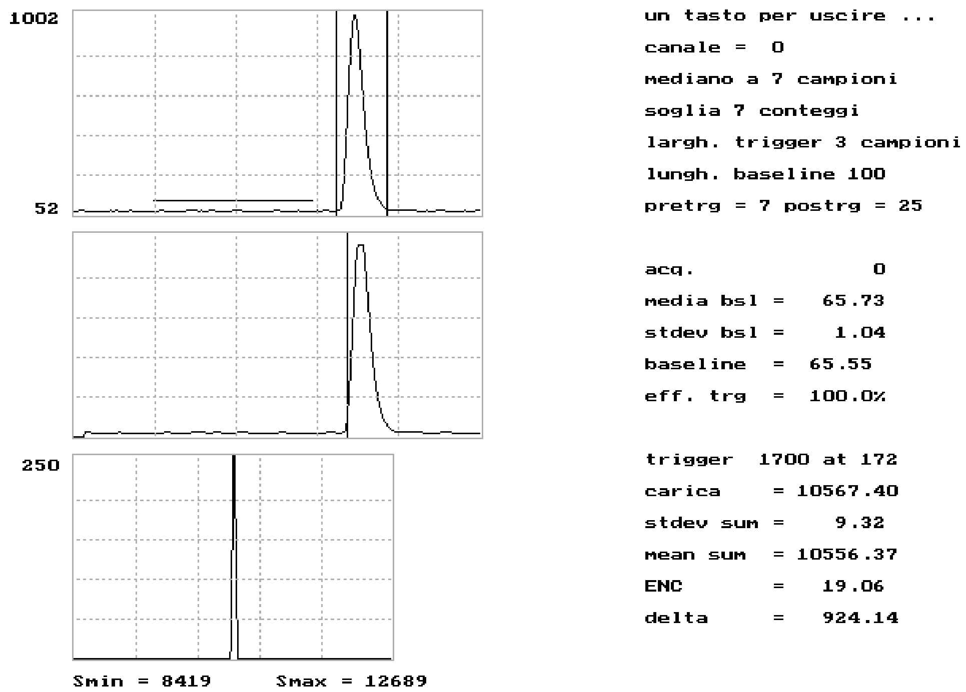

Fig.12 – Data elaboration with *300 fC* input signal

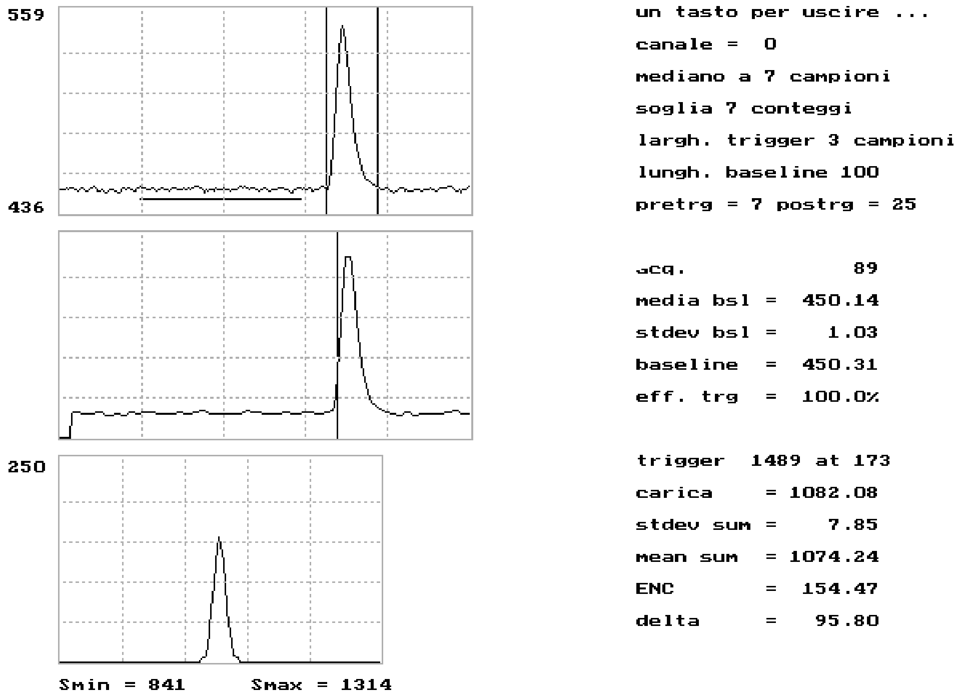

Fig.13 - Data elaboration with *30 fC* input signal

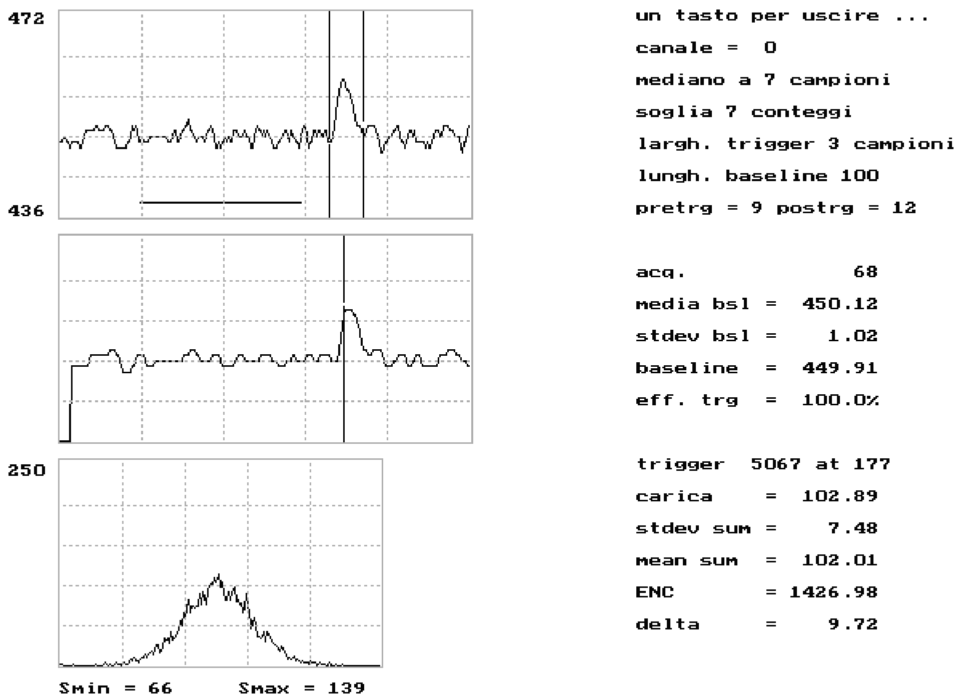

Fig.14 - Data elaboration with *3 fC* input signal

As introduced previously, the gain of the analog-digital conversion stage can be obtained by the ratio between the signal at the output of the analog channel (*872 mV*, please refer to Fig. 9) and the value of the **delta** displayed by the programme (*924.14 count*, please refer to Fig. 12), i.e.:

$$872\ mV / 924.14\ count = 0.94\ mV/count$$

As far as the signal-to-noise ratio S/N is concerned, two different cases must be addressed:

1) S/N in current,
2) S/N in charge.

The S/N in **current** is important as for the correct operation of the trigger and can be calculated by dividing the **delta** obtained with the *3 fC* input signal by the relevant value **stdev bsl**.

With reference to the figure 14 we obtain:

$$S/N_{current} = 9.72\ count / 1.02\ count = \mathbf{9.53}$$

The S/N in **charge,** i.e. after the numeric sum, is fundamental in order to reconstruct exactly the charge released in the detector and can be calculated by dividing the minimum electron charge injected by the **ENC** value.

With reference to the figure 14 we obtain:

$$S/N_{charge} = 18750\ e / 1427\ e = \mathbf{13.1}$$

According to the specifications, this figure must be greater than 10 (requirement for the collection planes) with a *400 pF* detector capacitance. Please note that, for the sake of easiness, this measurement was performed by using a *390 pF* SMD capacitance but, as it will be shown in the next chapter, if a Cd equal to *440 pF* is used, this requirement is still thoroughly fulfilled.

7. Performances versus detector capacitance

The noise performances versus the detector capacitance were measured on the channels 4 and 6 of the V791 board n. 2.

The channel 4 is equipped with two BF861B-type J-FET Philips @$I_D = 3.8\ mA$ each, while the channel 6 is equipped with two IF4500-type J-FET Interfet with the same drain current.

COG ceramic capacitors were used in order to simulate the detector: these capacitors were assembled in a traditional way and inserted, in turn, in a couple of contact pins soldered on the pad reserved for the third J-FET.

The sequence of capacitance values is equal to that suggested by P. Cennini in the Annex 3 of the Technical Specification document:

0, 100 pF, 220 pF, 440 pF, 820 pF

The results are displayed in Table 1.

C_d	ENC IF4500	σ IF4500	$COUNT_{max}$ IF4500	ENC BF861B	σ BF861B	$COUNT_{max}$ BF861B
0	*1037*	*0.66*	*9.61*	*992*	*0.56*	*9.27*
100 pF	*1094*	*0.69*	*9.50*	*1043*	*0.64*	*9.15*
220 pF	*1146*	*0.78*	*9.35*	*1259*	*0.80*	*9.19*
440 pF	*1299*	*0.90*	*9.22*	*1721*	*1.09*	*9.05*
820 pF	*1652*	*1.15*	*9.12*	*2534*	*1.54*	*8.97*

Tab.1 – Noise measurements vs detector capacitance

Figures 15 and 16 show the trends of ENC and of S/N in current as a function of the detector capacitance, respectively. The two curves refer to the two types of J-FET used.

Up to capacitances of about *500 pF* both the types are suitable although the IF4500 components definitely show a better performance as the detector capacitance increases. Please note that, on the other hand, the cost of the BF861B components is thoroughly lower.

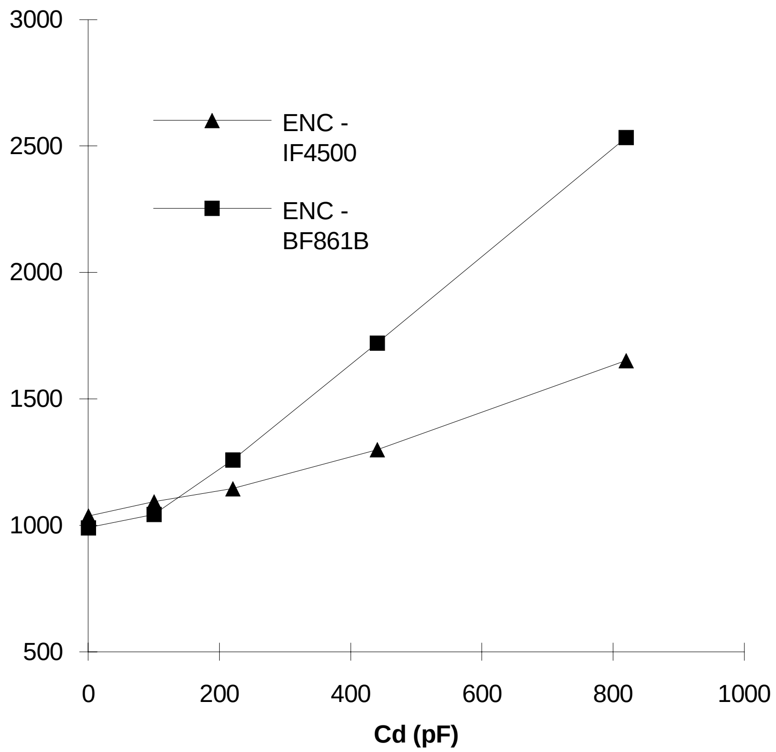

Fig.15 - ENC vs detector capacitance

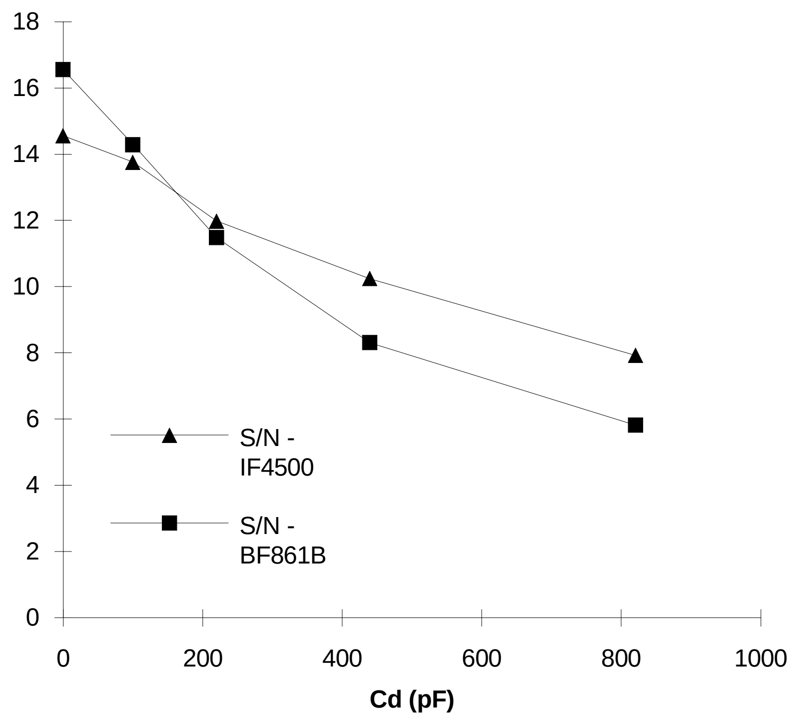

Fig.16 –The ratio S/N in current vs detector capacitance

8. Crosstalk

The crosstalk measurements were performed by driving, in turn, the test lines (even and odd) with the maximum signal.

During the test *390-pF* ceramic SMD detector capacitances were placed at the inputs of all the channels.

The measured crosstalk of the even channels on the odd ones was about *10%* and that of the odd channels on the even ones was less than *0.4%*.

It has been verified that there is a capacitive coupling of the preamplifier outputs of the even channels through the inputs of the odd ones. This is due to two reasons:

- a wrong location of the output connections of the even channels
- supposed wrong layer sorting of the layers of the printed board

The proposed solution consists in adding two further layers to the Printed Circuit Board (PCB), both connected to the ground, which encompass the layer containing the output connections of the preamplifiers in the same way as in a coaxial cable. This solution has been verified on the board n. 1. The output connection of the preamplifier of the channel 26 has been insulated and then the connection has been made again with a coaxial cable. In this way, by driving the channel 26 with the test signal, the maximum crosstalk to the other channels was *0.4%*.

The analog multiplexer too causes a crosstalk less than *0.4%* which can be found by taking into account the proper sampling sequence, i.e. two adjacent channels belonging to the same digitising subgroup (please refer to figure 1 of the Technical Specifications).

9. Notes on the trigger efficiency

The off-line trigger efficiency is 100% up to a detector capacitance greater than *440 pF* if the IF4500 components are used; if the BF861B ones are used, the off-line trigger efficiency is 100% up to a detector capacitance greater than *220 pF*. This is underlined in the figures from 17 to 26 of the Appendix.

The on-line trigger efficiency (*DAEDALUS* Chip) can be measured in the following by using a suitable set-up.

10. Appendix

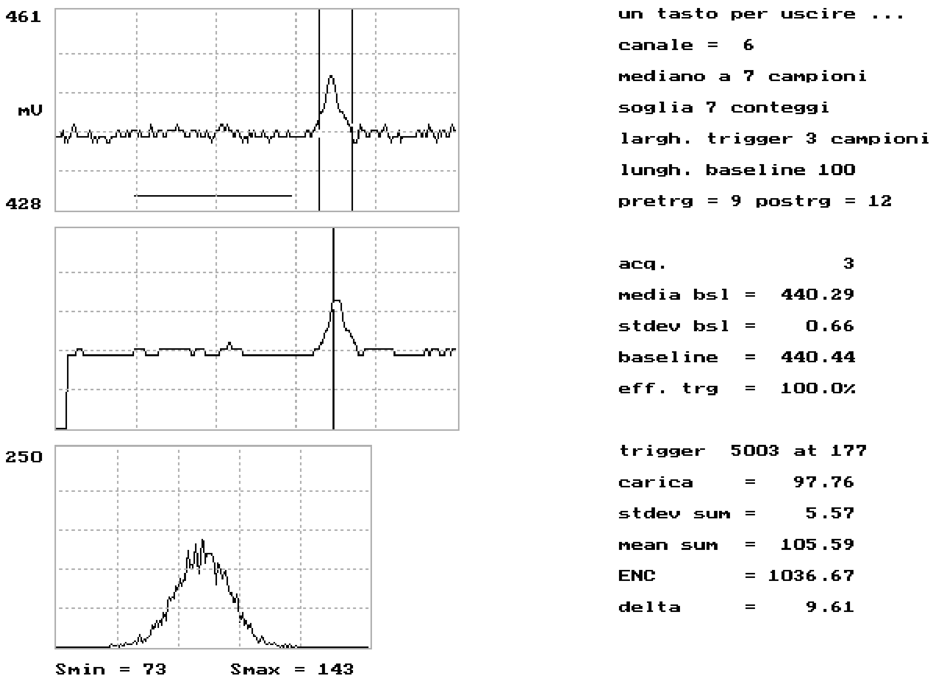

Fig.17 - Analysis of the channel 6 with *Cd = 0 pF,* IF4500, *Qi = 3 fC*

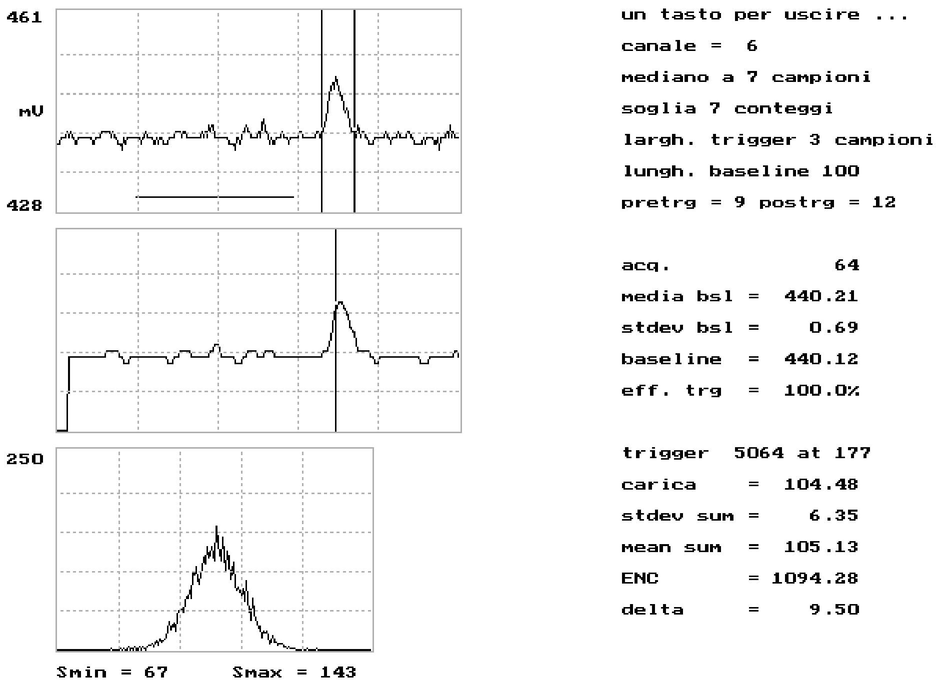

Fig.18 - Analysis of the channel 6 with *Cd = 100 pF,* IF4500, *Qi = 3 fC*

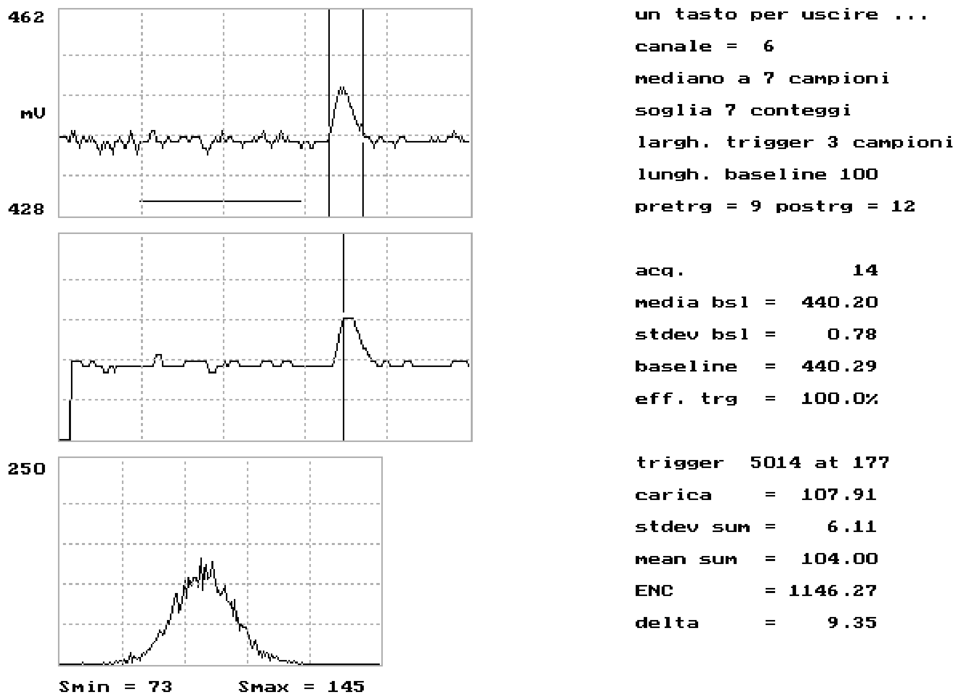

Fig.19 - Analysis of the channel 6 with *Cd = 220 pF,* IF4500, *Qi = 3 fC*

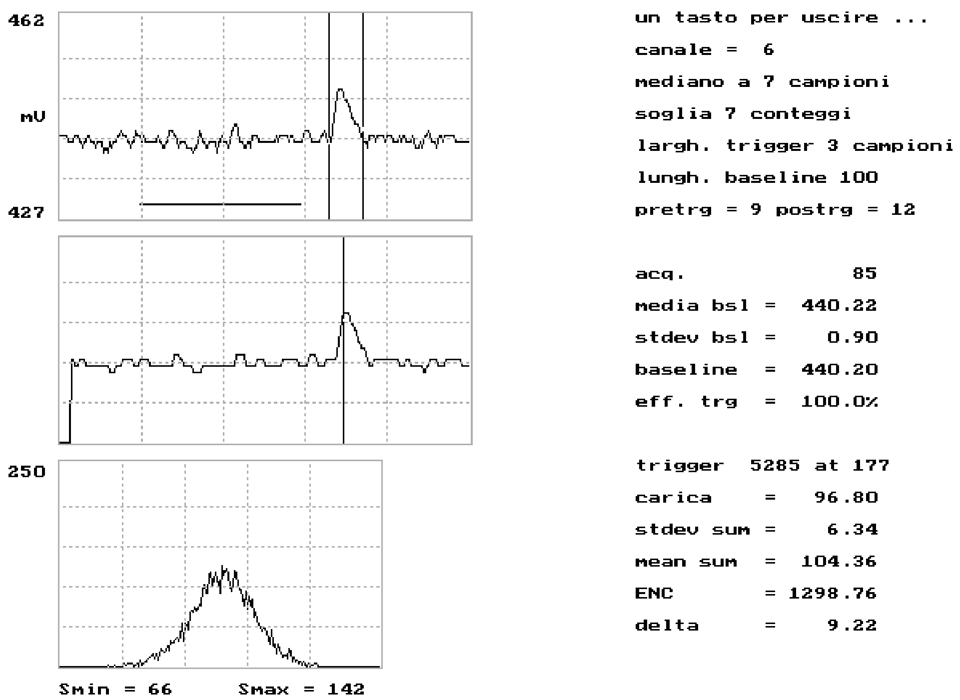

Fig.20 - Analysis of the channel 6 with *Cd = 440 pF,* IF4500, *Qi = 3 fC*

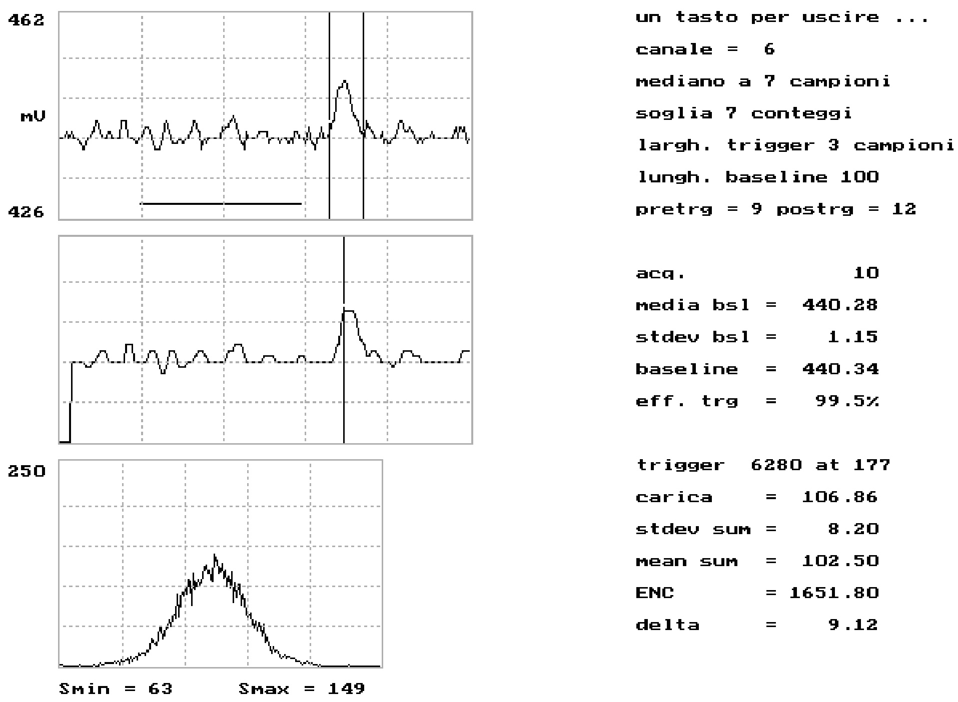

Fig.21 - Analysis of the channel 6 with *Cd = 820 pF,* IF4500, *Qi = 3 fC*

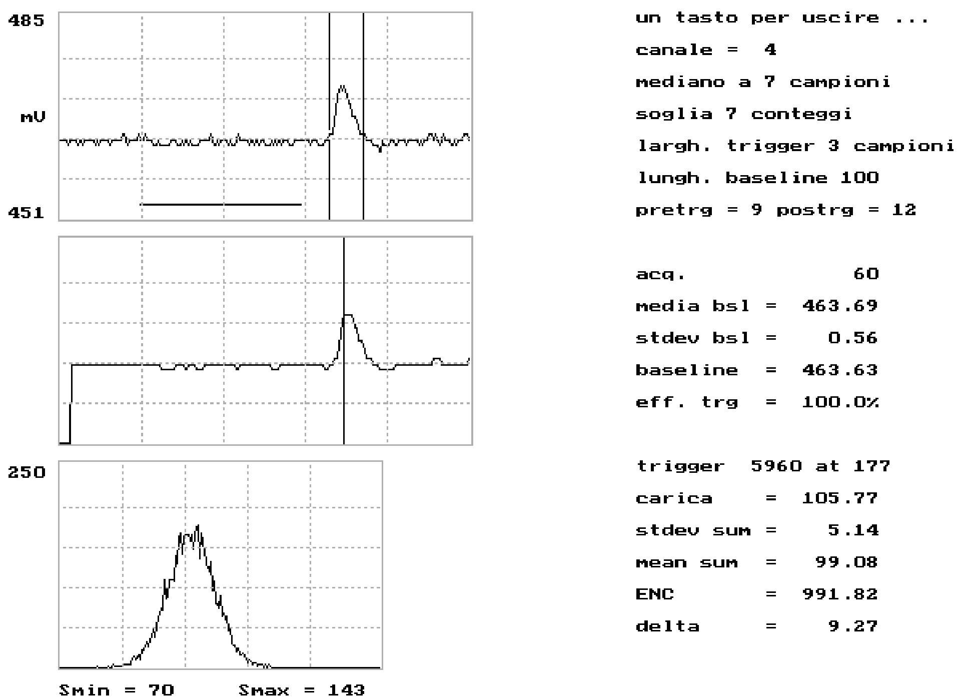

Fig.22 - Analysis of the channel 4 with *Cd = 0 pF,* BF861B, *Qi = 3 fC*

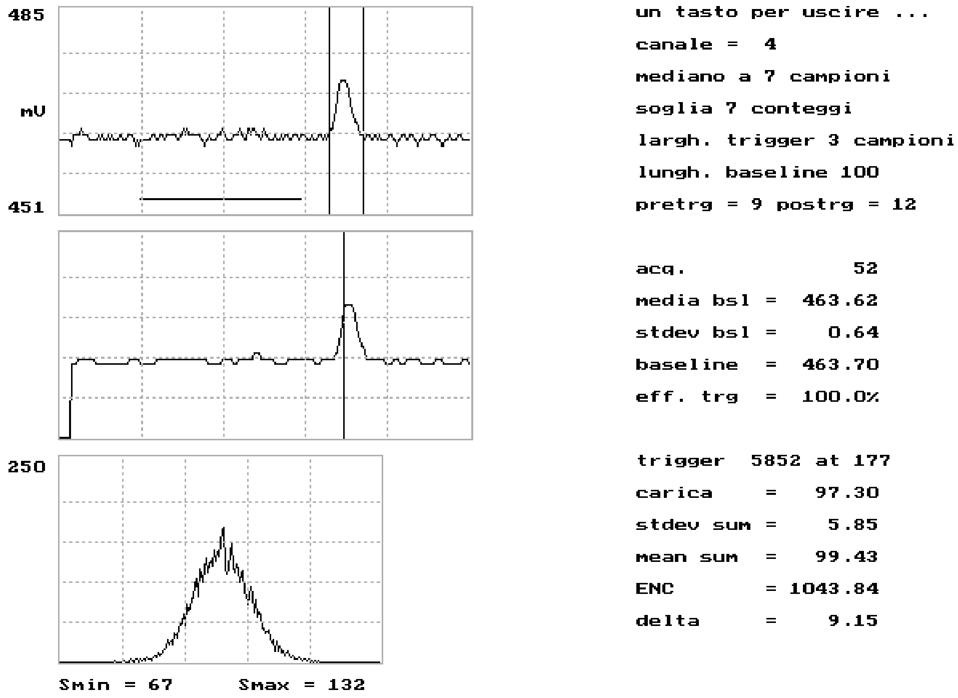

Fig.23 - Analysis of the channel 4 with *Cd = 100 pF,* BF861B, *Qi = 3 fC*

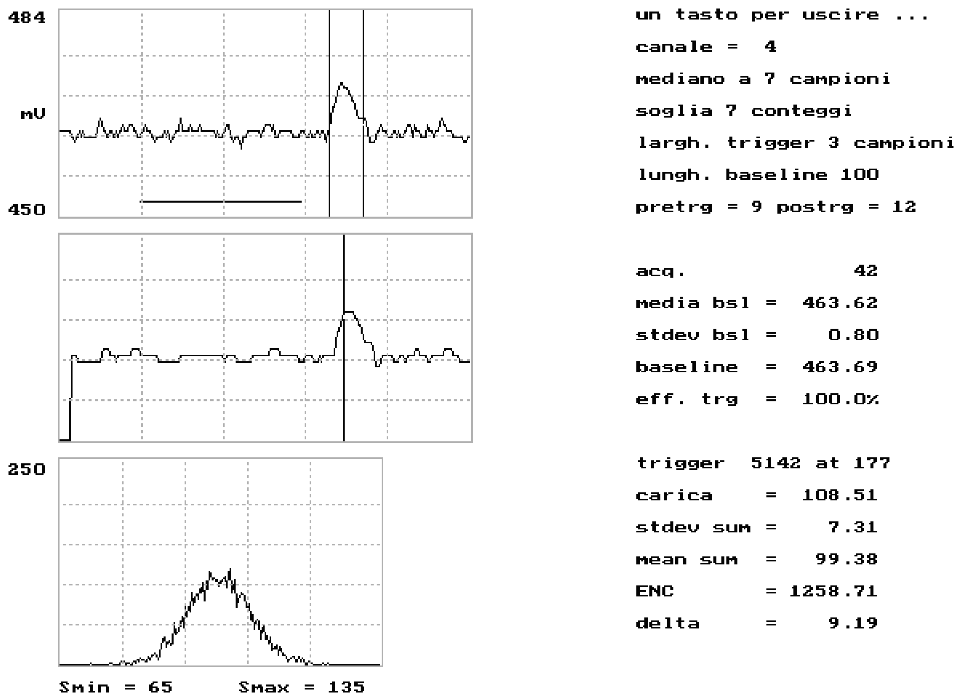

Fig.24 - Analysis of the channel 4 with *Cd = 220 pF,* BF861B, *Qi = 3 fC*

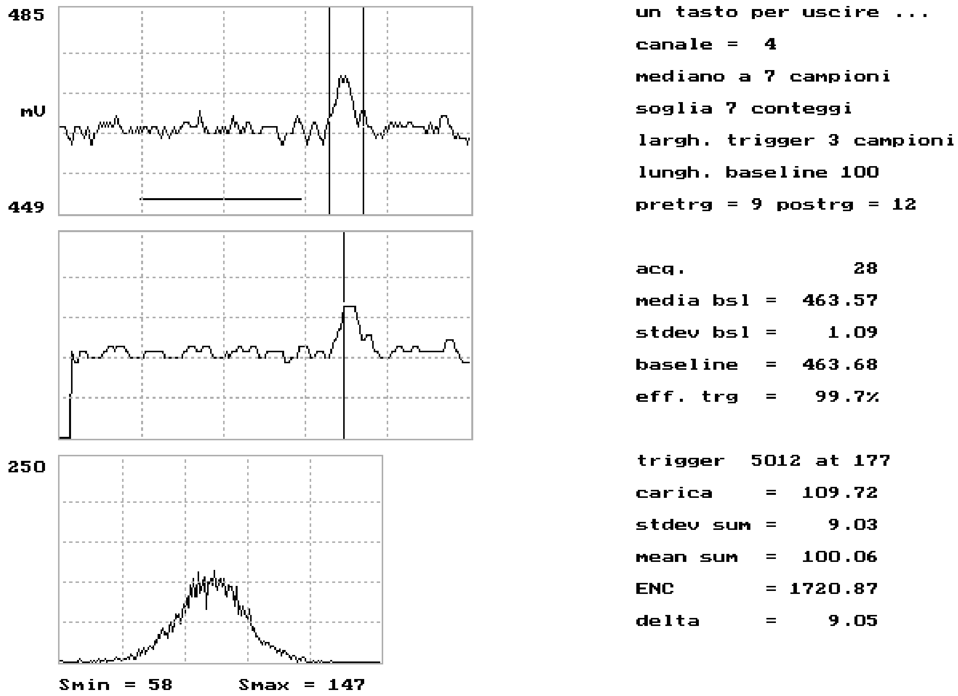

Fig.25 - Analysis of the channel 4 with *Cd = 440 pF,* BF861B, *Qi = 3 fC*

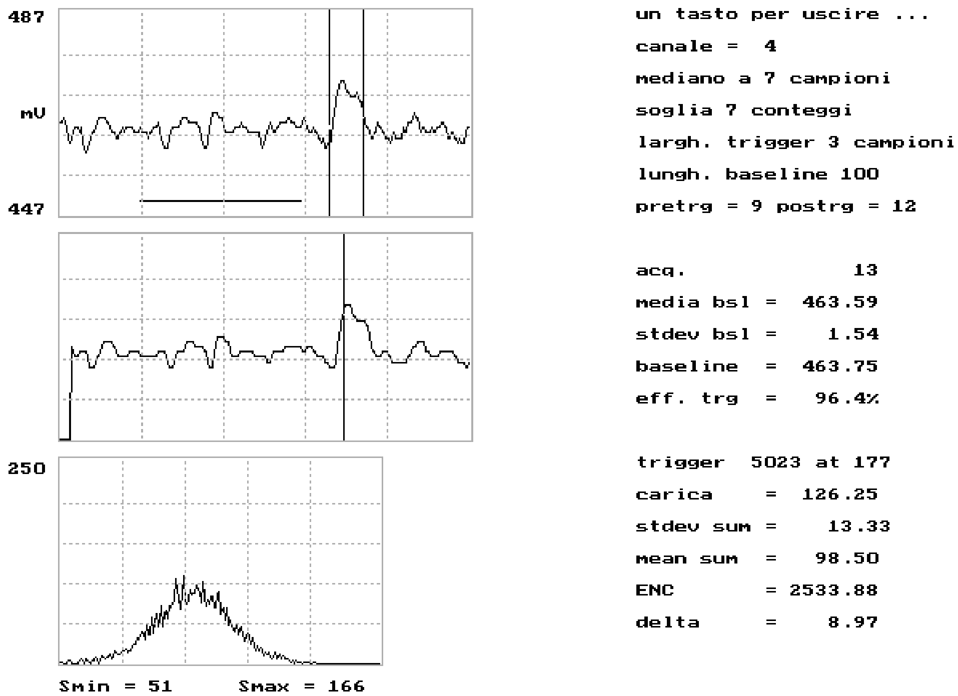

Fig.26 - Analysis of the channel 4 with *Cd = 820 pF,* BF861B, *Qi = 3 fC*